REMARKS

In the Office Action, the Examiner:

- rejected Claims 1, 4-7, 10-17, and 20-23 under 35 U.S.C. 102(e) as being unpatentable over Bristow et al. (US Patent No. 6,754868 B2);
- objected to Claims 2-3, 8-9 and 18-19 as being dependent upon a rejected base claim, but indicated that the claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In this amendment, Claims 1, 7, and 17 have been amended to more clearly distinguish the claimed invention from Bristow. After entry of this amendment, the pending Claims will be 1-23. Support for the above claim amendments can be found throughout the originally filed specification, drawings, and claims. Entry of the amendment and reconsideration of rejected claims are respectfully requested.

Claim 1 as amended recites:

> An apparatus for testing a device under test (DUT) having a plurality of pins, the apparatus comprising:
>
> a clock having a clock cycle
>
> a plurality of pin electronics channels (PEs) capable of coupling to the plurality of pins on the DUT;
>
> a plurality of timing and format circuits (T/Fs) each capable of mapping a signal to one of the plurality of PEs;
>
> a pattern memory capable of storing a number of bits for testing the DUT, the pattern memory having a plurality of outputs capable of outputting the bits to test the DUT; and
>
> a pattern scrambler coupled between the plurality of outputs and the plurality of T/Fs, the pattern scrambler capable of being programmed to couple bit from any one or more of the plurality of outputs to any one or more of the plurality of T/Fs, to provide a test pattern to the DUT having a programmable width from 1 bit wide to a width equal to the number of the plurality of PEs.

Claim 1 as amended is patentable over Bristow because Bristow does not disclose an apparatus for testing a DUT comprising, among other things, a pattern scrambler coupled between a plurality of outputs and a plurality of T/Fs and capable of being programmed to couple any of the plurality of outputs to any one or more of the plurality of T/Fs, to provide a test pattern having a programmable width. Bristow does not provide a pattern scrambler. The pin scrambling circuit (155) in Bristow is not a pattern scrambler and does not possess the

functionalities and/or capabilities of the pattern scrambler in Claim 1 as amended. For example, the pin scrambling circuit (155) in Bristow cannot be programmed to couple any of the plurality of outputs from the pattern memory to any one or more of the plurality of T/Fs. As shown in FIG. 4 of Bristow, output for Pin 1 from the logic vector memory (175) is hardwired to scrambler 180 coupled to the T/F (150) for Pin 1, ... and output for Pin n from the logic vector memory (175) is hardwired to scrambler 180 coupled to the T/F (150) for Pin n (Col. 6, lines 40-44 and lines 53-57, and FIGS. 3 and 4). Therefore, the pin scrambling circuit (155) in Bristow cannot be programmed to couple any of the outputs (such as the output from pin n) from logic vector memory (175) to any of the T/Fs (150) (such as the T/F connected to pin 1).

Furthermore, the pin scrambling circuit (155) in Bristow does not provide a test pattern having a programmable width. As shown in FIG. 4, each pin scrambler (180) in the pin scrambling circuit (155) outputs a fixed number of (3) bits per clock cycle and there are a fixed number of (n) pin scramblers (180). Thus, the total number of bits output from the pin scrambling circuit (155) is fixed and not programmable. In contrast, because the claimed invention allows any of the plurality of outputs from the pattern memory to be coupled to any one or more of the T/Fs, multiple sets of T/Fs can be coupled to a same set of outputs selected from the plurality of outputs, and the data pattern to each set of the T/Fs can have a programmable width equal to the number of T/Fs in the set, which number can be from one to the number of the plurality of PEs. This allows the apparatus in Claim 1 to be used to test multiple identical DUTs in parallel (p. 17, lines 14 – p. 18, line 4 in the Specification).

Therefore, Claim 1 as amended is patentable over Bristow.

Claims 2-6 depend from Claim 1 and are patentable for the same reasons as Claim 1 and by reason of the additional limitations set forth therein.

The arguments regarding Claim 1 applies to Claim 7 as amended. Therefore, Claim 7 should also be patentable.

Claims 8-16 depend from Claim 7 and are patentable for the same reasons as Claim 7 and by reason of the additional limitations set forth therein.

Claim 17 as amended recites:

A method for testing a device under test (DUT) using a test system including a

pattern memory having a plurality of outputs equal to *n*, and a pattern scrambler coupled between the plurality of outputs and a plurality of pins on the DUT, the method comprising steps of:

storing a number of bits for testing the DUT in the pattern memory; and

programming the pattern scrambler to select, for each pin of the DUT, one or more bits from all of the plurality of outputs to be coupled to one or more of the plurality of pins on the DUT, and to provide a test pattern to the DUT having a programmable width of from 1 to *n* bits.

Claim 17 as amended is patentable over Bristow because Bristow does not disclose a method for testing a device under test comprising, among other things, the step of programming the pattern scrambler to select, for each pin of the DUT, one or more bits from all of the plurality of outputs of the pattern memory, and to provide a test pattern to the DUT having a width of from 1 to *n* bits. As discussed above, Bristow does not provide a pattern scrambler, and the pin scrambling circuit (155) in Bristow cannot be programmed to select, for each pin of the DUT, one or more bits from all of the outputs of the logic vector memory (175) because these outputs are hardwired to respective scramblers 180 coupled to respective T/Fs (150) for respective pins (115) of the DUT. Therefore, Claim 17 as amended is patentable over Bristow.

Claims 18-23 depend from Claim 17 and are patentable for the same reasons as Claim 17 and by reason of the additional limitations set forth therein.

Prompt and favorable consideration of this Amendment and Response is respectfully requested. If the Examiner believes, for any reason, that personal communication will expedite prosecution of the application, the Examiner is invited to call the undersigned at (650) 494-8700.

Respectfully submitted,

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